Model 1612P

Single Board PCM Data System

Third Generation real-time 0-40 Mbps Telemetry Decom "all-in-one" Processor

Single card Bit Sync, IRIG Time, Decom, PCM Sim, CVSD, 8 ch DAC

Program driven card level "soft- decom" real-time TM processor

Acroamatics Telemetry System Software (ATSS) included - Lifetime Support!

Includes IADS Server and integrated TMATS import

Up to ten stream system configurations

IRIG Chpt 4 , 5 (CVSD) & 8 PCM processing

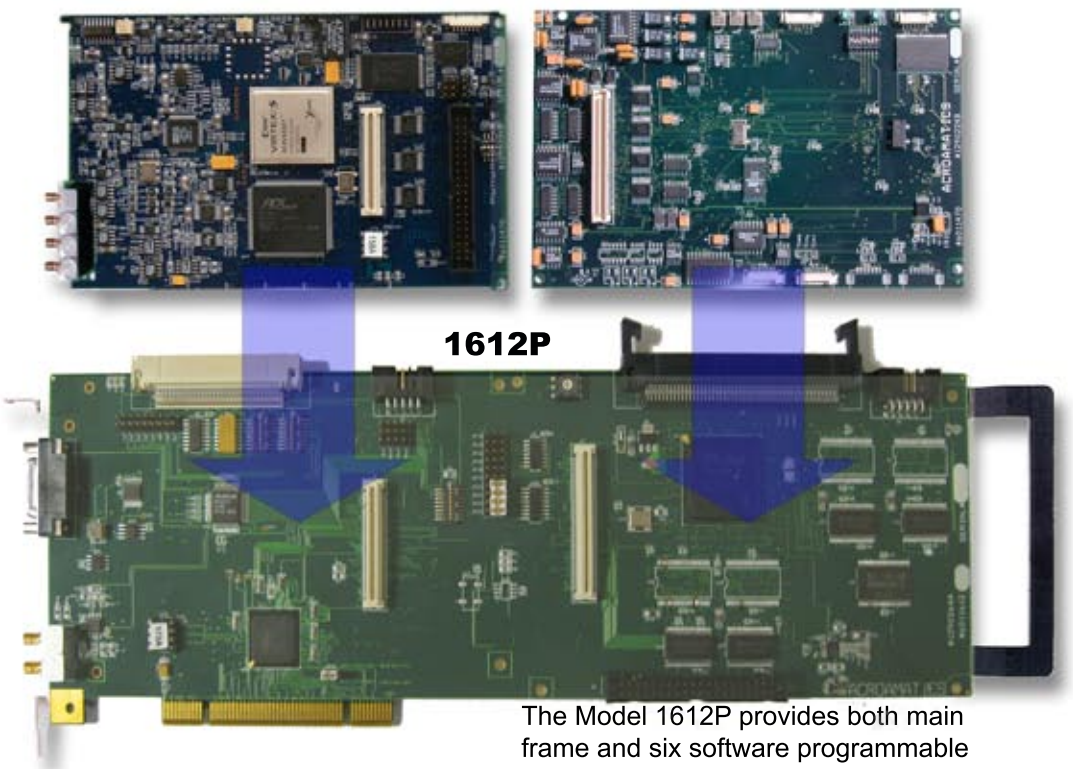
NASA CCSDS & packet TM decommutation

Embedded Async Format Processing

Model 474DM Tunable High Performance Digital Bit Sync

Model 470M IRIG A/B/G time Reader / Generator

0- 64 Mbps Programmable PCM Simulator & Output Reconstructor



The newly designed Model 1612P features higher data rate and processing speeds and many new capabilities, yet retains 100% "drop-in" compatibility with existing Acroamatics PCI TDP products and systems. We've utilized the latest in PGA component technology to deliver both low power (1/3 of the Model 1602P Decom) and improved reliability - ensuring users trouble-free, upgrade friendly systems for the next decade.

We've added lots of new features to the new 1612P too, including new features to enable users and integrators to more easily interconnect optional onboard bit syncs, additional 1612P decoms, and our powerful PCI 1605P TM data merger / real-time telemetry data processor.

Most importantly, the new 1612P retains our signature card level,real-time stored program processing technology.

The Model 1612P provides both main frame and six software programmable "soft decom" driven sub-frame decommutators - each with multiple onboard data and conditional stored memory program locations. Though the 1612P PCI decom operates wholly independent of Windows, it is designed to allow use of standard Windows driven PCI bus and system processes to independently record data to disk, drive Windows display processes, and share data over network connections - making it a very effective stand alone all-in-one telemetry processing device.

Used as part of an integrated multi-stream real-time telemetry processing solution, any number of independent 1612P cards operate in conjunction (sharing time and status info). When joined with our companion 1605P PCI PDSP module real-time results any eight 1612P modules in the system may be used to drive a wide range of complex output data processes - all processing events remaining 100% Windows independent and deterministic.

ACROAMATICS

TELEMETRY SYSTEMS

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Model 1612P PCI Single Board Data System

FUNCTION

Sources	Program selectable, one of four inputs: three NRZ-L. Data and 0º Clock inputs; one internal Test Pattern input.
Impedance	50 Ohm input impedance, TTL compatible.
Bit Rate	Up to 40 M bits per second.
Polarity	Programmable, automatic polarity correction.
Word Length	Programmable, 1 to 32 bit word length for each input.
Word Orientation	Programmable, MSB/LSB orientation for each input word.
Parity	Selectable leading, trailing, or no parity checking for each word.

SYNCHRONIZATION

Mainframe Sync	Mainframe synchronization provides for programmable synch pattern and mask, complement pattern recognition, and variable length frame decommutation. The pattern may be up to 64 bits in length.
Subframe Sync	Six independent synchronizers are capable of decommutating sub-frames within subframes. Subframes synchronize to fixed recycle patterns, complement frame sync patterns, and various ID patterns. Both recycle and ID patterns may be assembled from multiple word locations. Recycle patterns may be up to 32 bits long.
ID Sync	Two types of ID synchronization are supported: JAM patterns of arbitrary values, and incrementing or decrementing frame counters with limit checking. ID sync words may be up to 16 bits in length.
Sync Strategy	Programmable Search-Check-Lock sync strategy, bit error tolerance,and bit slip window provide reliable frame synchronization.
Asynchronous Formats	Subframe synchronizer may be programmed to decommutate embedded formats having unique frame sync patterns and format structures.
Format Switching	16 testable flags store the results of bit or word comparisons on the input stream to control decommutation.

OUTPUTS

Standalone Data Output	Data is available to the host computers PCI bus as memory-mapped frame buffers, Current Value Table (CVT), or as a data stream selectably transferred by PCI bus DMA. Data is 32 bits with programmable MSB/LSB output word justification, sign extension, or zero insertion for LSB output. Acroamatics Telemetry System Software (ATSS) suite provides a host of Windows compatible (XP and Windows 7 compatible) shich support user decom set-up, mission set-up management, and a host of real-time data display, alarming, recording, discrete/analog, and networked data I/O processes and local operator status display, and remote system management and data operations support.
I-Buss Data Output	When used in a system configured with a 1605P PCI level advanced telemetry processing module,the primary output of the Model 1612P uses a 64 bit parallel inter-card bus connection called “I-bus”, that processes messages containing thirty-two bits of data, twelve bits of fine time (microseconds), two bits of status, and 17 bits of data identification. The output data can be in either MSBor LSB-justified form. LSB-justified data can also be sign extended. The data messages are transmitted via the I-bus to the 1605P resident Distribution & algorithmic data processor. Data is then buffered and queued for output to the 1605P Programmable Data Stream Processor section for further processing. The 1605P is capable of merging data from up any of up to to eight 1612P cards in a system, selectively processing the data for real-time analog (DAC) outputs, and freal-time, deterministic formatting of data for seelect format recording, real-time display, and networked data communications.
Frame Quality	Frame quality word is generated containing bit sync and frame sync status for downstream data validation.
2 Serial PCM Outputs	Two programmably controlled RS-422 compatible serial output channels are supported.
CVSD Audio	IRIG Ch 5 CVSD or PCM encoded digital audio format decommutated audio output. Utilizes one of eight DAC channels (below)
DAC	Eight independent, program assignable 12-bit D-to-A channels capable of reproducing select word or paramater data.

PCM SIMULATOR

Bit Rate	to 64 Mbps
Programming	Automatically copies word and frame attributes from programmed Decom setup or for more sophisticated simulator setups Text file programming is provided.
Data Sources	1024 Static Registers, Two User-Defined 16 bit Dynamic Data Memories, Two 16-bit Modulo Up/Down Counters, 16-bit Pseudo-Random Generator, 16-bit Program Counter
Word Lengths	Programmable for each data source Static data words range from 1 to 32 bits All other data sources range from 1 to 16 bits
Word Orientation	Programmable MSB/LSB for each data word
Dynamic Data Memory	2K x 16 bit RAM, Pre-settable to ramp, sine, triangle or square wave functions
Frame Length	Maximum of 4096 words

OUTPUT

Internal	Internally connects to Bit Synchronizer or Frame synchronizer via program control
Clock and Data	Zero degree Clock, NRZ-L data, TTL
PCM Code Type	Sixteen selectable output codes: NRZ-L/M/S, Bi □-L/M/S, DBi □-M/S, DM-M/S, MDM-M/S, RNRZ 11, 15, 17 and 23

OPTONS

Tunable Bit Synchronizer	The Model 474DM 8 Hz to 40 MHz Advanced Digital Bit Sync Mezzanine Module may be ordered with or added to the 1612P.
IRIG Time Code	One Model 470M IRIG Time Reader/Generator / PCM Sim Mezzanine is required per system for real-time IRIG time sync.

PHYSICAL

Format	Standard PCI: full length single slot
Cooling Requirements	30 Linear FPM
Power Requirements	+3.3VDC at 3.0 Amps, (including optioal mezzanine bit sync and / or time modules)
Dimensions	4.20” (10.67cm) H x 12.5” (31.75cm) W x .55” (1.4cm) D
Temperature	Operating: 0º to +40º C, Non-Operating: -40º to +86º C
Relative Humidity	Up to 90% non-condensing
Shock Operating	Operating: 6G, Non-Operating: 50G
Vibration	Operating: 0.5G, 5 to 2000Hz, Non-Operating: 1.2G, 5 to 500Hz

Specifications subject to change without notice